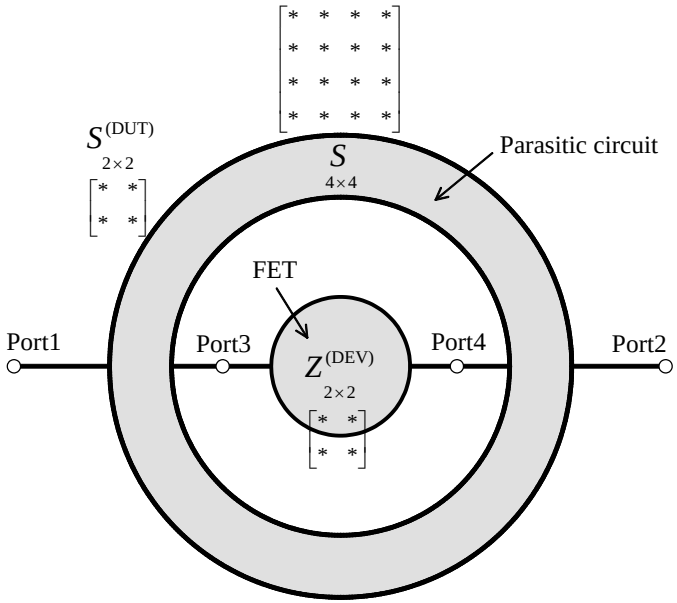
De-Embedding Method Using EM Simulator for Device Characterization



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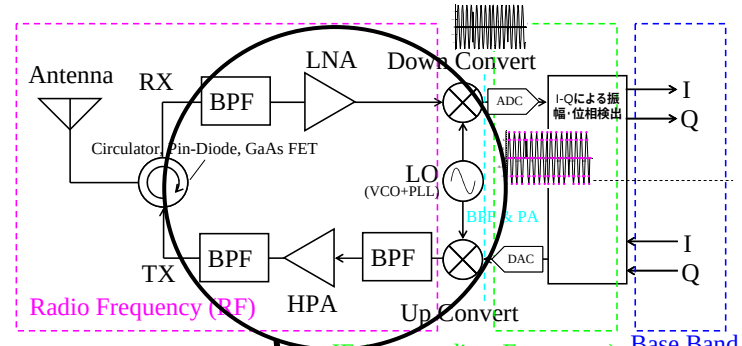
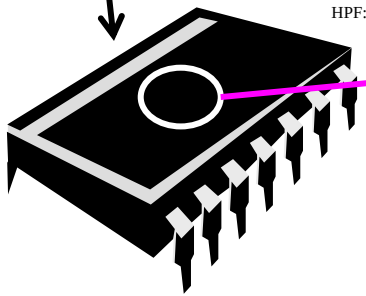
Background

Wireless Terminal



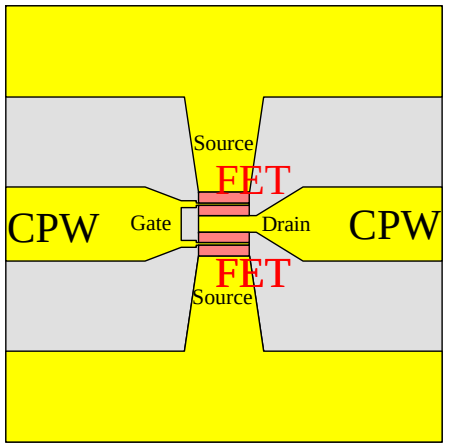
Architecture



Monolithic Microwave Integrated Circuit (MMIC)

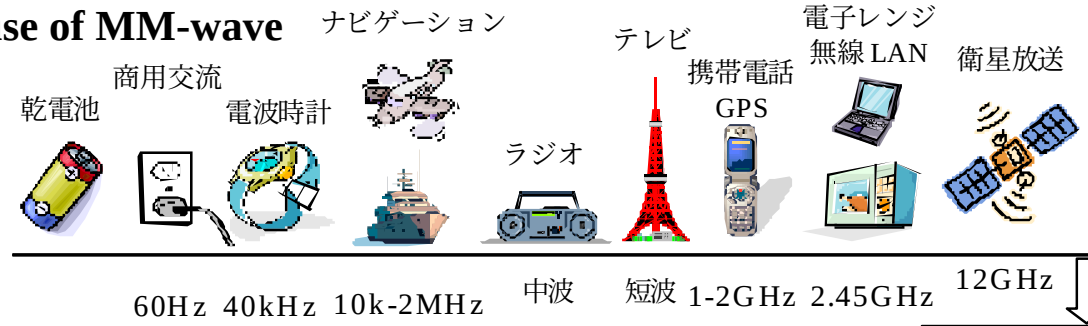
FET is a leading part.

High accuracy characterization is necessary



Test Element Group (TEG)

For public use of MM-wave

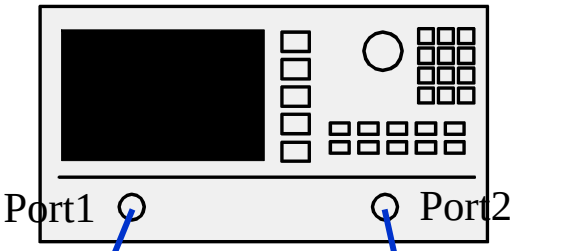


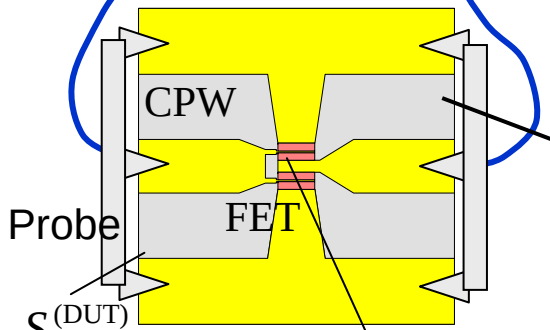
RF Si CMOS in MM-wave
Characterization of FET

Very difficult

Objective

Vector Network Analyzer (VNA)





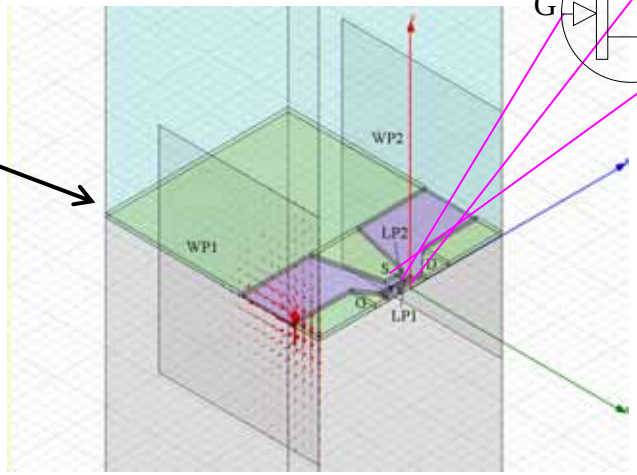
$S_{ij}^{(DUT)}$ (2×2) TEG $Z_{ij}^{(DEV)}$ (2×2)

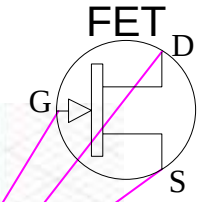
Measured by VNA

Unknown

De-embedding (Remove the effect of the parasitic circuit, and extract that of the FET.)

TEG

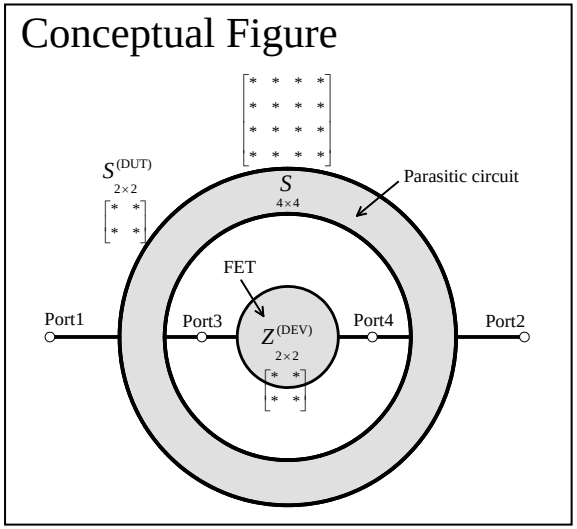




S_{ij} (4×4)

EM Analysis

Conceptual Figure

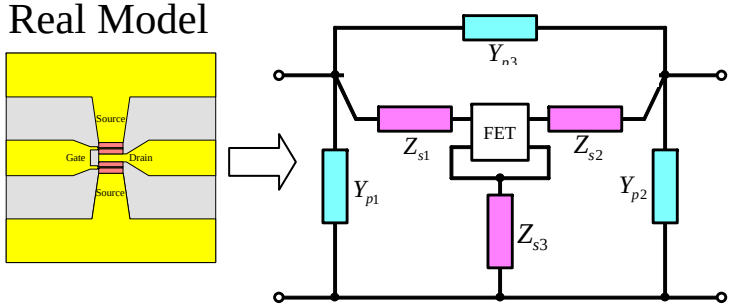


Conventional Method and Its Problem

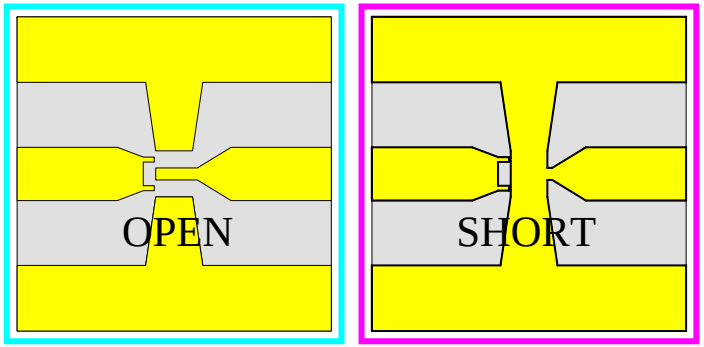
	Conv. method
Approx.	Equiv. Circuit ⇩ Is the topology enough? (?)
Ambiguity	Experiment Are open/short pattern accurate? (?)
Generality	Every time when TEG pattern is changed, we are worry about the methodology. (?)

Equiv. Circuit

Real Model



Is this approx. valid?



Used to remove parasitic circuit in the equiv. circuit model.

Are there really open and short?

$I = 0 \qquad V = 0$

Procedure of the Proposed Method

(i) Calibrate VNA, and measure 2-port DUT S-parameters.

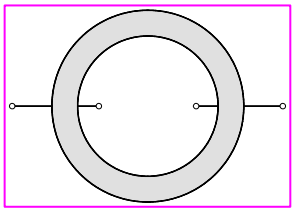
(ii) Analyze 4-port S-parameters of parasitic circuit using EM simulator.

(iii) Convert the S-parameters of the parasitic circuit into hybrid A-parameters, in which Port3 and 4 are treated as lumped parameters. New

(iv) Extract 2-port parameters of the lumped element by matrix algebra.

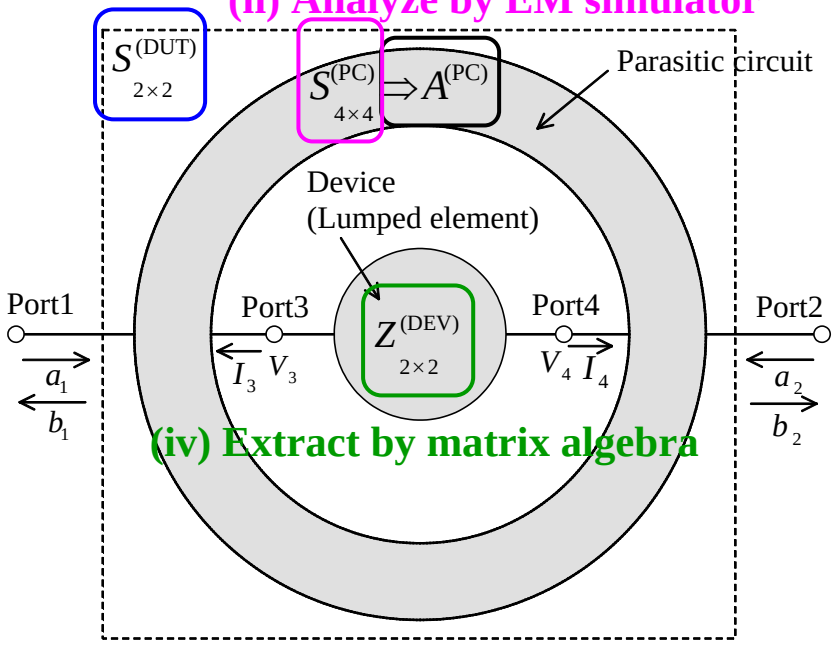
De-embedding method using EM simulator

c.f.) S. Bousnina et al., IEEE Trans. MTT, vol.50, no.2, pp.420-424, Feb. 2002.

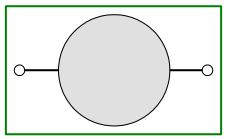


(i) Measure by VNA

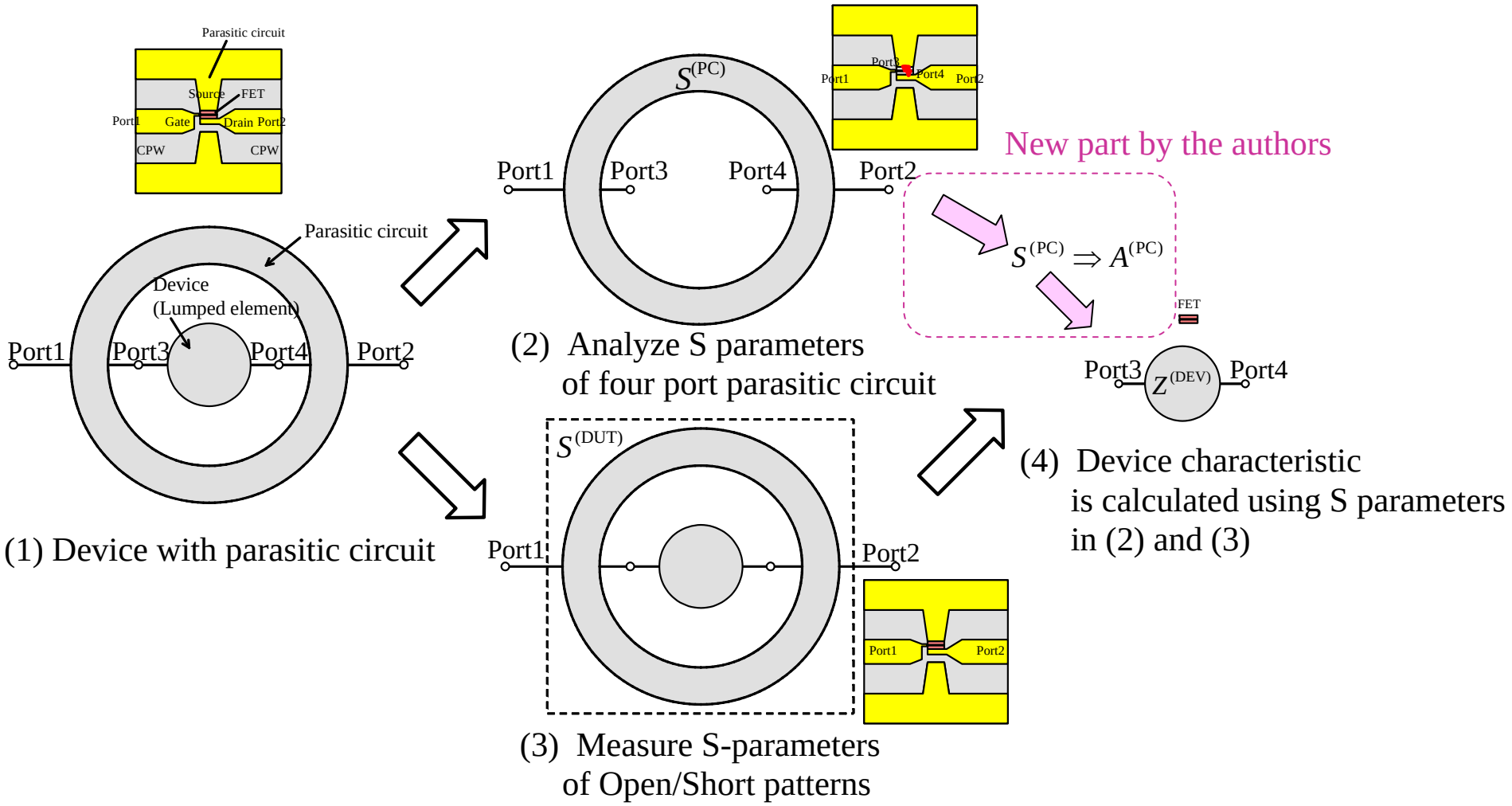
(ii) Analyze by EM simulator



(iv) Extract by matrix algebra

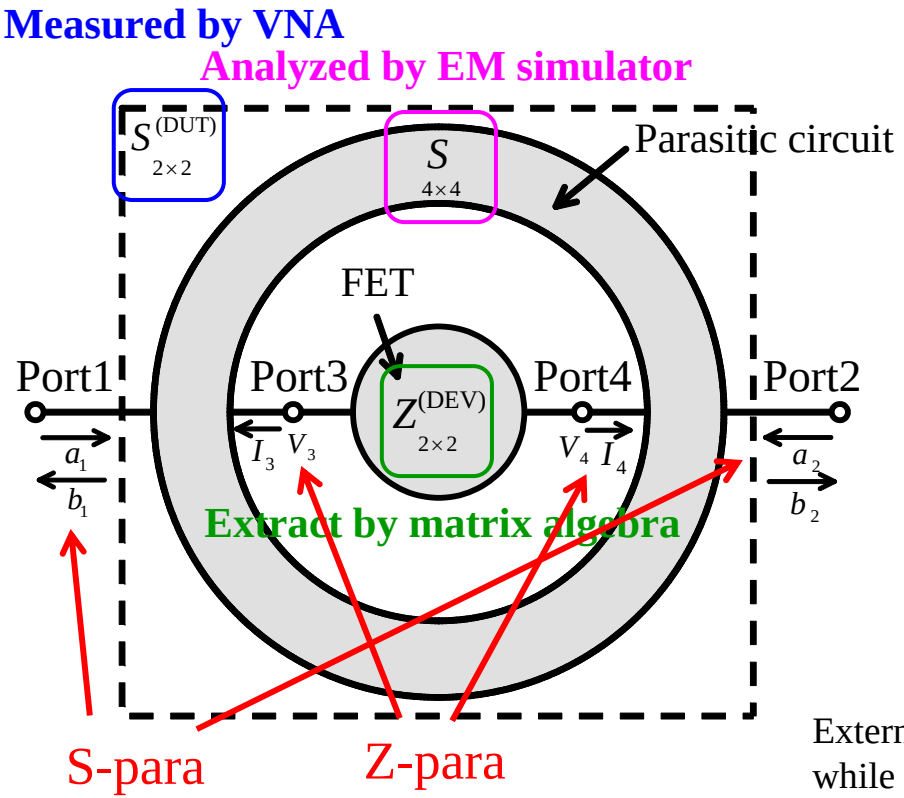


Conceptual Flow of the Proposed Method



c.f.) S. Bousnina et al., IEEE Trans. MTT, vol.50, no.2, pp.420-424, Feb. 2002.

Step (iv): Extraction of FET parameter by Matrix Algebra



Step (iii)

$$\begin{bmatrix} b_1 \\ b_2 \\ V_3 \\ V_4 \end{bmatrix} = \left[\begin{array}{cc:cc} A_{11} & A_{12} & A_{13} & A_{14} \\ A_{21} & A_{22} & A_{23} & A_{24} \\ \hdashline A_{31} & A_{32} & A_{33} & A_{34} \\ A_{41} & A_{42} & A_{43} & A_{44} \end{array}\right] \begin{bmatrix} a_1 \\ a_2 \\ I_3 \\ I_4 \end{bmatrix} = \left[\begin{array}{c:c} A_{\{11\}} & A_{\{12\}} \\ \hdashline A_{\{21\}} & A_{\{22\}} \end{array}\right] \begin{bmatrix} a_1 \\ a_2 \\ I_3 \\ I_4 \end{bmatrix} = A \begin{bmatrix} a_1 \\ a_2 \\ I_3 \\ I_4 \end{bmatrix}$$

$$\begin{cases} A_{\{11\}} = S_{\{11\}} + S_{\{12\}}\left(I - S_{\{22\}}\right)^{-1} S_{\{21\}} \\ A_{\{12\}} = \dfrac{S_{\{12\}}\left[\left(I - S_{\{22\}}\right)^{-1}\left(I + S_{\{22\}}\right) + I\right]\mathrm{diag}(\sqrt{Z_3}, \sqrt{Z_4})}{2} \\ A_{\{21\}} = 2\,\mathrm{diag}(\sqrt{Z_3}, \sqrt{Z_4})\left(I - S_{\{22\}}\right)^{-1} S_{\{21\}} \\ A_{\{22\}} = \mathrm{diag}(\sqrt{Z_3}, \sqrt{Z_4})\left(I - S_{\{22\}}\right)^{-1}\left(I + S_{\{22\}}\right)\mathrm{diag}(\sqrt{Z_3}, \sqrt{Z_4}) \end{cases}$$

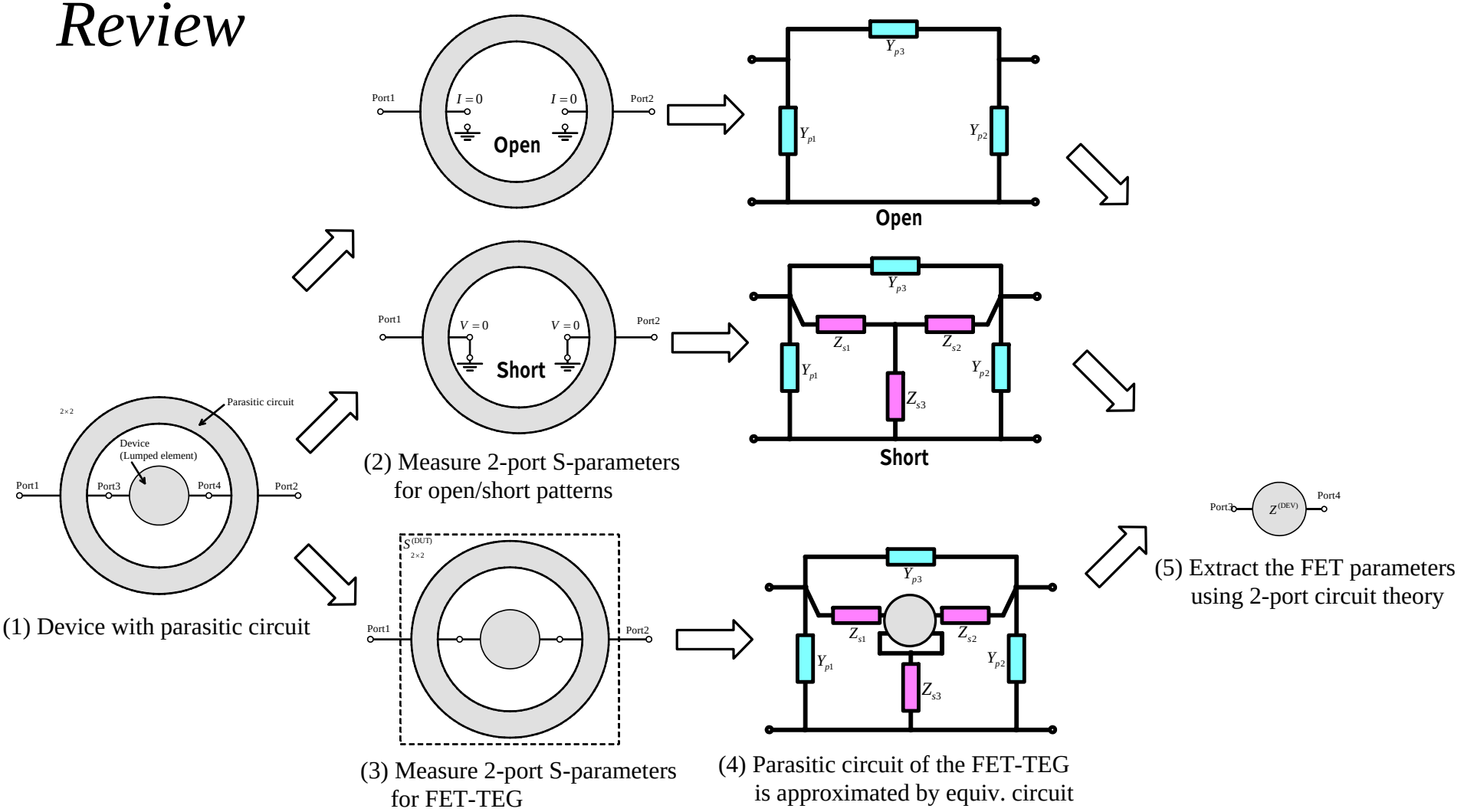
External ports are expressed by S-parameters
while inner ports are expressed by Z and/or Y parameters.
⇨ Characteristic impedances of external ports are not necessary.

Step (iv)

$$Z^{(DEV)} = -A_{\{21\}}\left(S^{(DUT)} - A_{\{11\}}\right)^{-1} A_{\{12\}} - A_{\{22\}}$$

Conceptual Flow of the Conventional Method

Review



(1) Device with parasitic circuit

(2) Measure 2-port S-parameters for open/short patterns

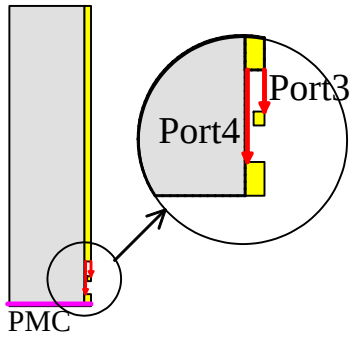
(3) Measure 2-port S-parameters for FET-TEG

(4) Parasitic circuit of the FET-TEG is approximated by equiv. circuit

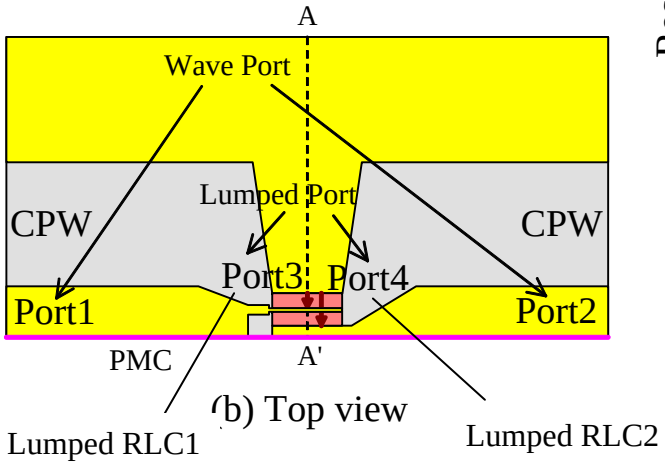
(5) Extract the FET parameters using 2-port circuit theory

c.f.) M.C.A.M. Koolen et al., Proc. IEEE, Bipolar/BiCMOS Circuits and Tech. Meeting, pp.188-191, Sept. 1991.

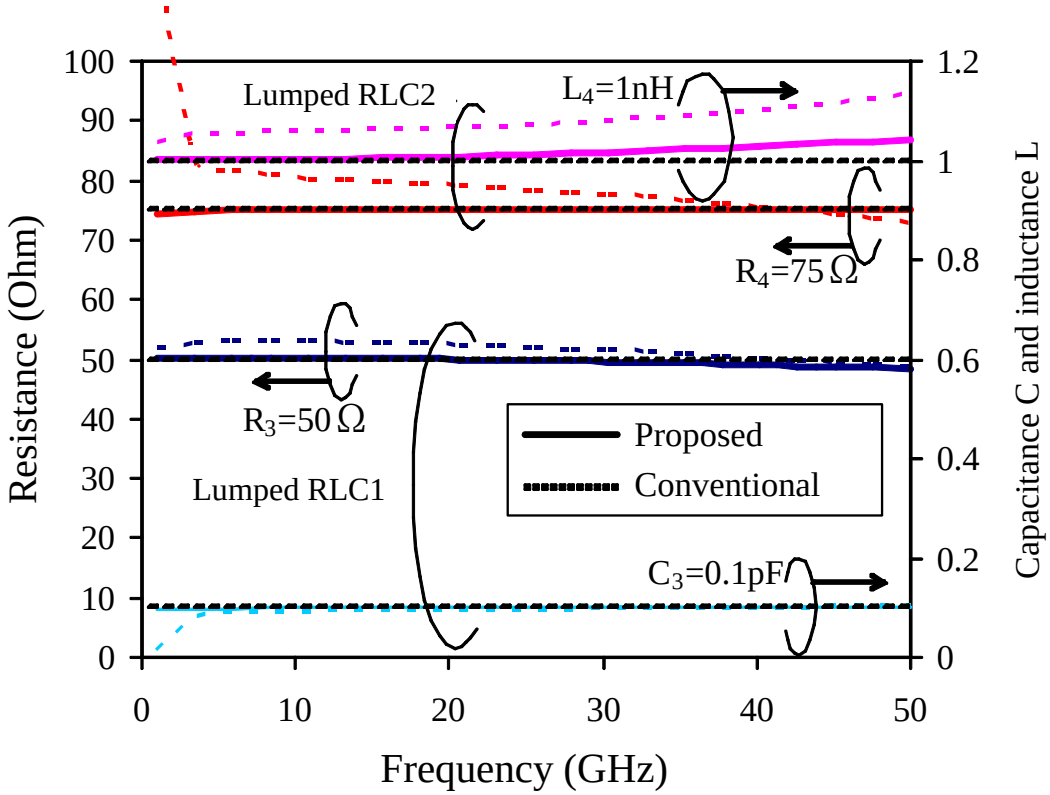
Numerical Simulation of De-embedding Method



(a) Cross-section at A-A'



(b) Top view



(c) Numerical simulation of deembedding

Accuracy of the proposed method is higher than the conventional method

Summary (1/2)

	Conv. method	Proposed method
Approx.	Equiv. Circuit Is the topology enough? (?) ✕	EM simulator TEG structure and mutual are considered completely! ○
Ambiguity	Experiment Are open/short pattern accurate? (?) ✕	EM simulator Is EM simulator accurate? Is fabricated TEG structure and material parameters accurate? ⇨ Confirmed by open/short-TEG ○
Generality	Every time when TEG pattern is changed, we are worry about the methodology. (?) ✕	Arbitrary-shaped TEG can be treated. Extension to N-port problem is easy. EMC, Inter-chip interference problem etc. ○

General, High accuracy

Conclusions (2/2)

Proposed method

- Proposed de-embedding method using EM simulator.
- 4-port S-parameters of the parasitic circuit is analyzed by the EM simulator (without equivalent circuit approx.).
- External ports are expressed by S-parameters while inner ports are expressed by Z and/or Y parameters.

Results

- Generality is high.
- Accuracy is higher than the conventional method.
- Primary error factor of the conventional method is identified to be approximation of parasitic circuit by the equivalent circuit.
- Applicable to lossy substrate.

Future tasks

- Experimental verification.
- Extension to N-port problem, EMC, inter-chip interference and so on.