Introduction of Direct Sampling Mixer with Low Noise Design

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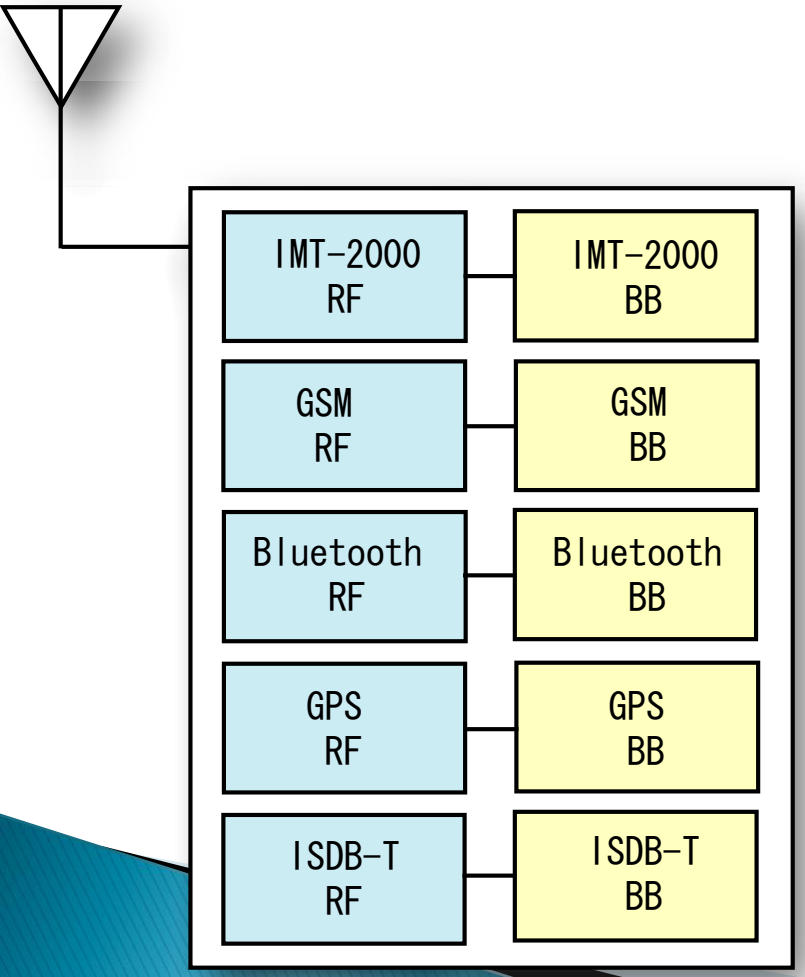
- Role of Mixer
- Classification of Mixer
- Introduction of Direct Sampling Mixer (DSM)
- Issues and Objectives
- Noise analysis of SCF networks
- Noise Figure (NF) of DSM
- Conclusion

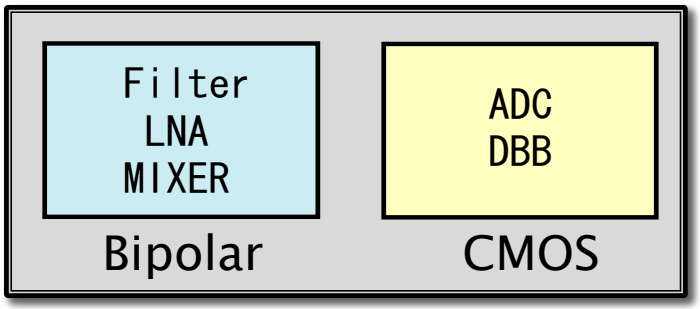
Background 1

Example of
receiver block in mobile terminal



- Receiver circuit is being designed for each standards.
- Receiver compose of different process.

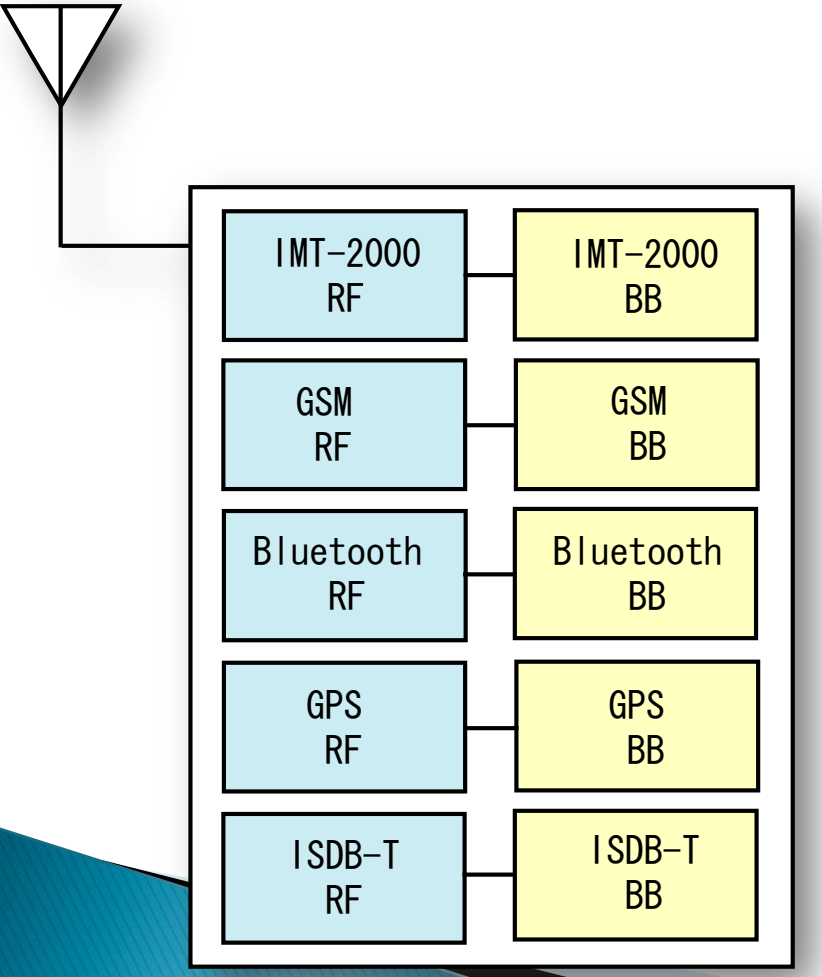
SiP(System in Package)



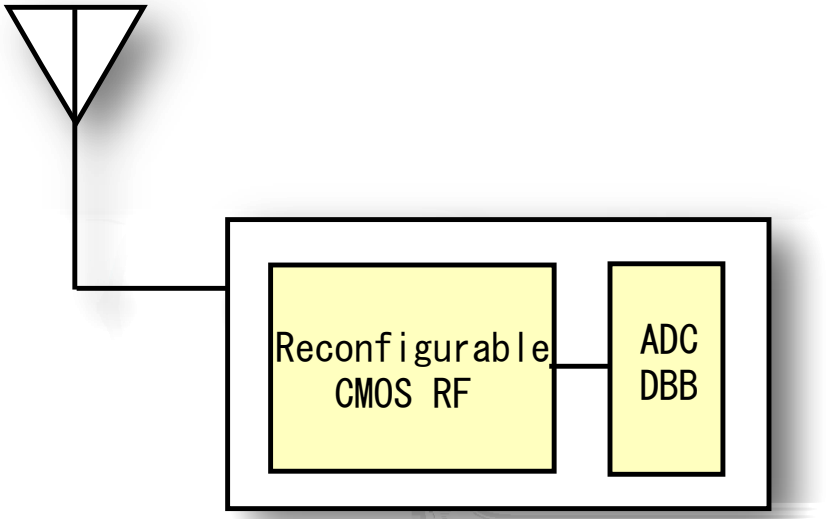
- big size
- high power consumption

Background 1

Example of
receiver block in mobile terminal



- Multi-standard CMOS 1 chip receiver is desired.



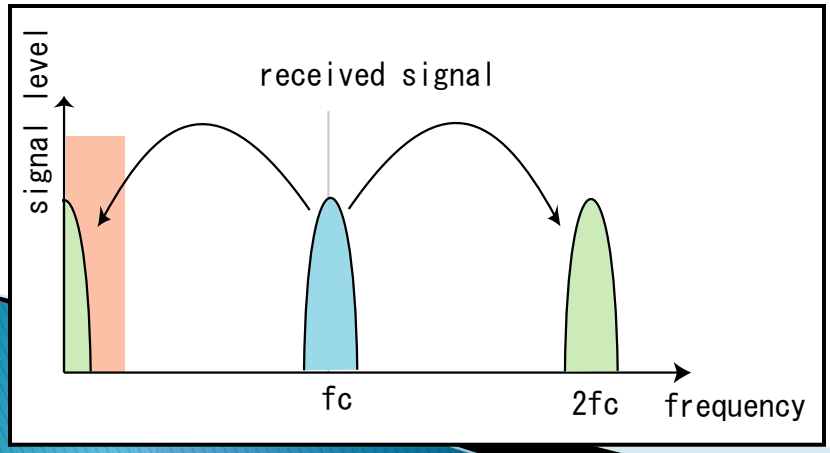
Background

- Requirements
  in wireless cc
  - Small s
  - Low p

receive

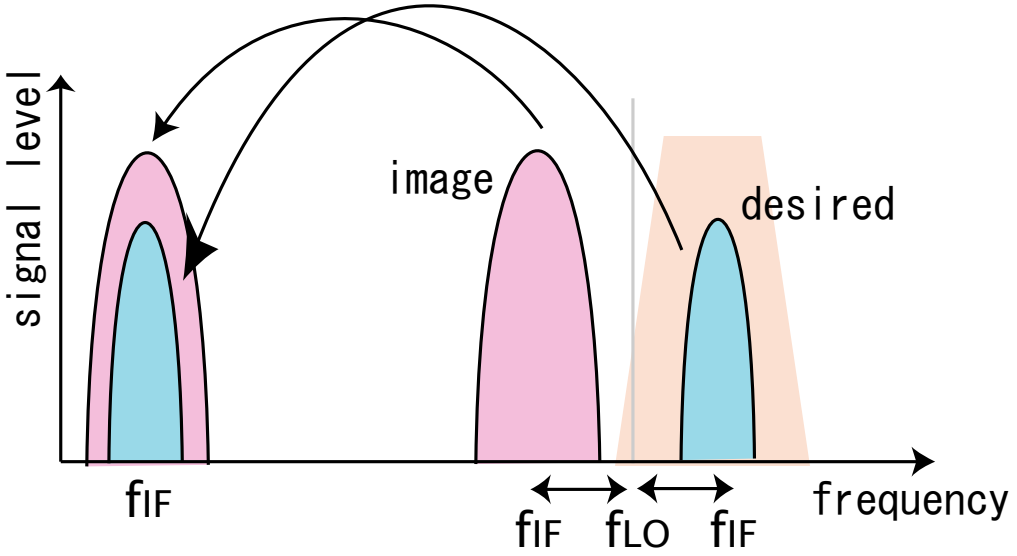
What is Mixer?

- In receiver, signal received at antenna is handed to ADC.
- In digital stage, transmitted information is demodulated.
- Information data is very low rate compared with carrier frequency.
- To reduce the operation rate of ADC, it is necessary to pick out only information from received signal. It is performed by mixer and filter.



Classification of Mixer 1

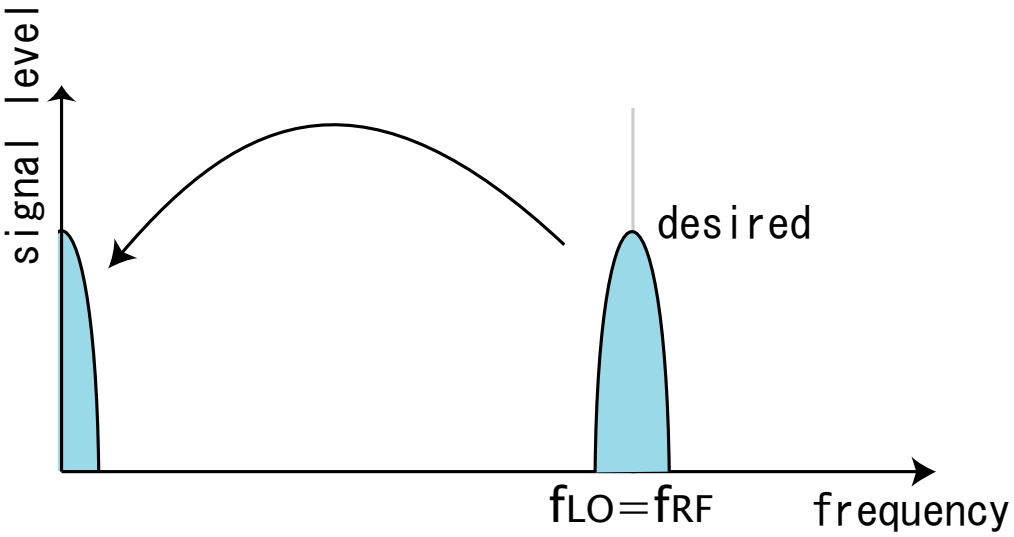
- ✓ Where is signal output?
- Intermediate Frequency (super heterodyne)
  - good performance
  - need image rejection in front of mixer



Classification of Mixer 1

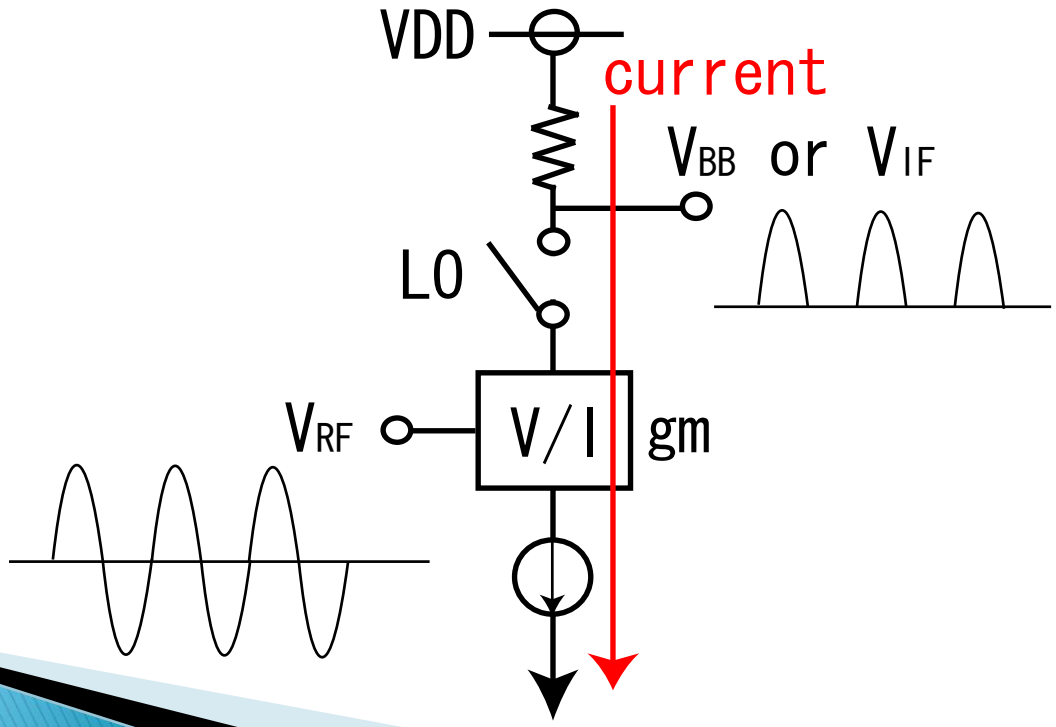
- ✓ Where is signal output?
- Intermediate Frequency (super heterodyne)
- Base Band (Direct-conversion)
  - not so good performance (DC offset, flicker noise)
  - no image

⇒ suitable for multi-standard receiver



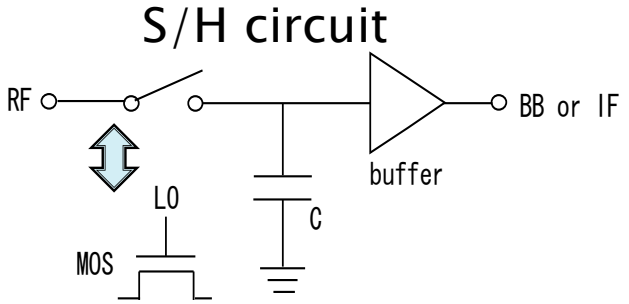
Classification of Mixer 2

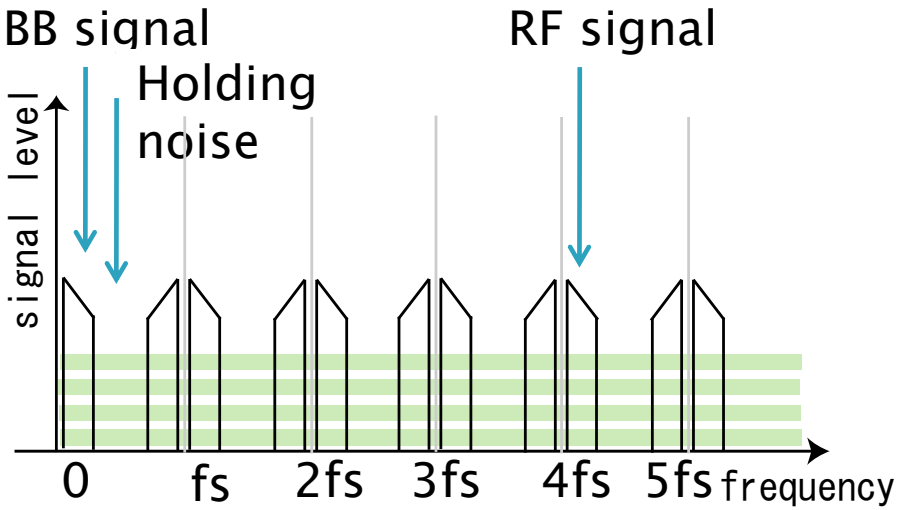
- How is down-conversion performed?
- Continuous time (Gilbert cell)
  - VDD can not be reduced.
  - Not suitable for CMOS technology



Classification of Mixer 2

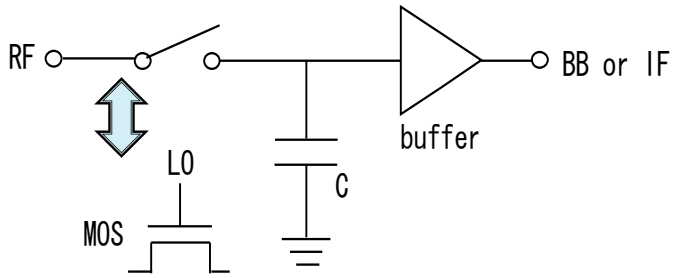
- How is down-conversion performed?
- Continuous time (Gilbert cell)
- Discrete time (Sampling mixer)
  - Sub sampling
    - MOS performs as a switch.
    - fLO=fRF/n (n: integer)
    - Fast switching operation is not needed.
    - Holding noise is big issue.



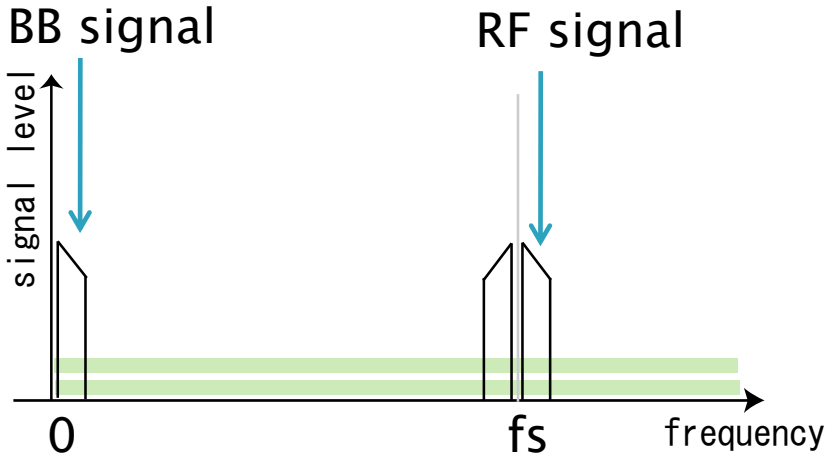


Classification of Mixer 2

- How is down-conversion performed?
- Continuous time (Gilbert cell)
- Discrete time (Sampling mixer)
  - RF sampling
    - fLO=fRF
    - CMOS in deep submicron technology can adapt to fast switching operation.
    - Holding noise can be reduced.



S/H circuit

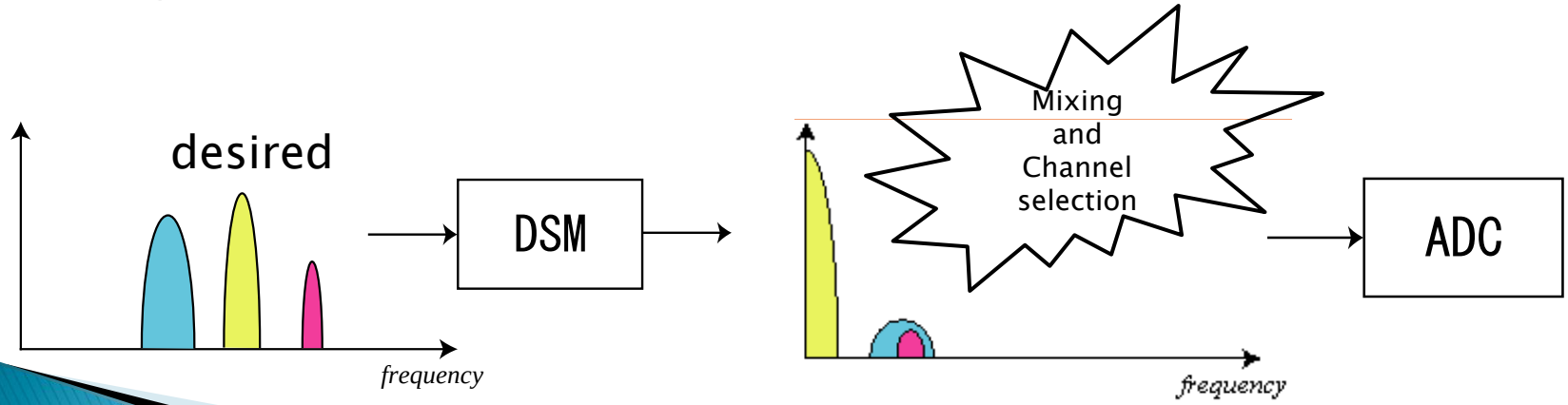


Classification of Mixer

- ✓ Direct Sampling Mixer (DSM)
- Where?
  - Direct-conversion
- How?
  - RF sampling

Suitable for multi-standard CMOS receiver

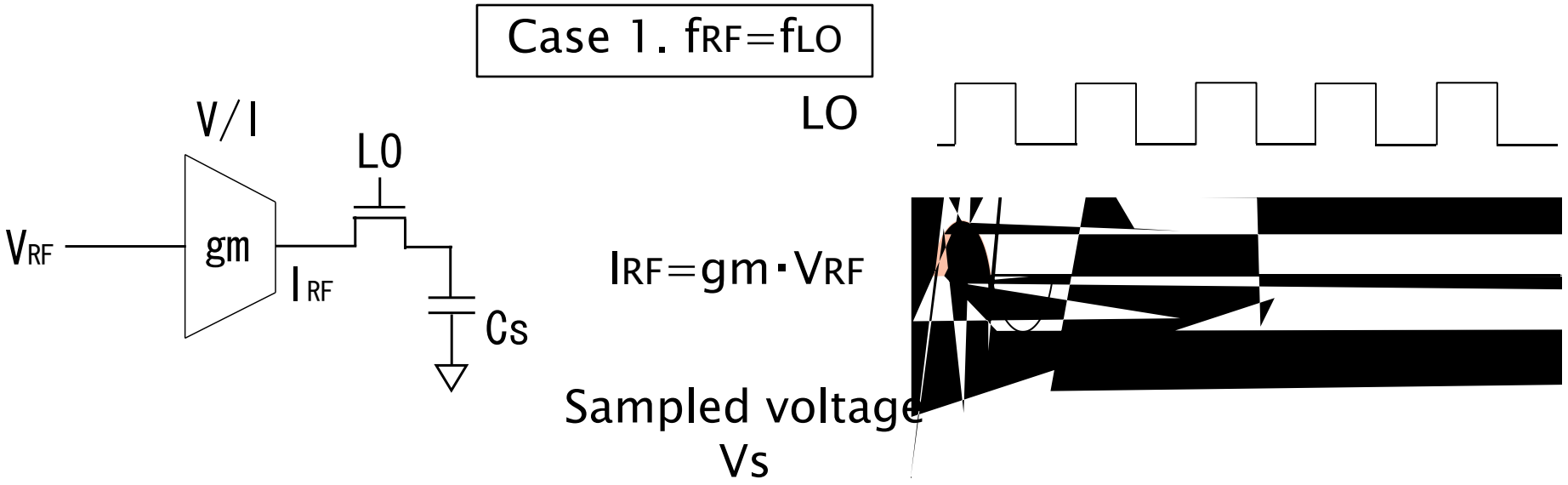
- DSM is Filter embedded mixer



can reduce power consumption

Current-Integration Sampling

- Input voltage is converted to current by transconductans amplifier.
- Cs integrates current.
- Integration window is controlled by clock LO.

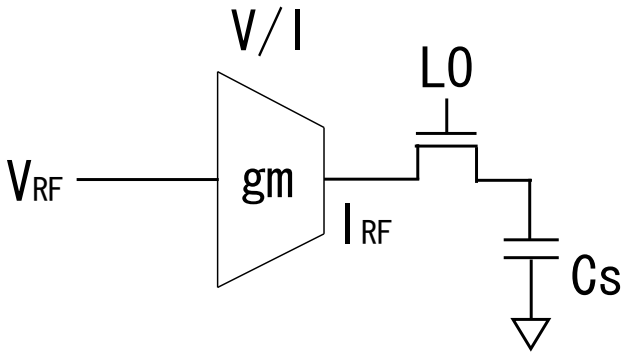


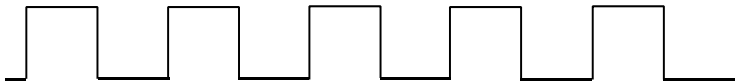
Desired RF signal is converted to DC.

Current-Integration Sampling

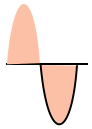
- Input voltage is converted to current by transconductans amplifier.
- Cs integrates current.
- Integration window is controlled by clock LO.

Case 2. $f_{RF}=2f_{LO}$





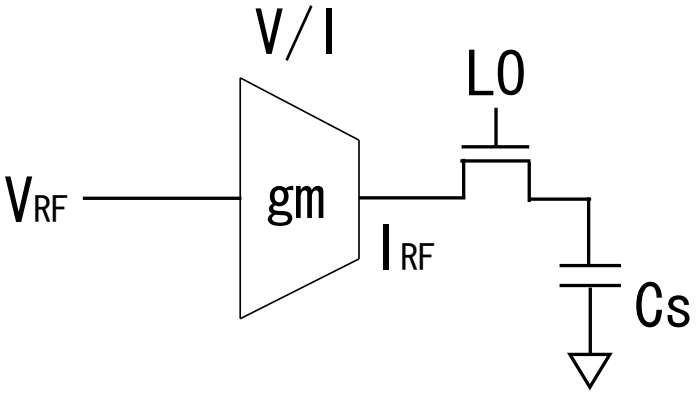
$I_{RF}=gm \cdot V_{RF}$



Sampled voltage
Vs

Interference (noise) signal at $2f_{LO}$ is suppressed.

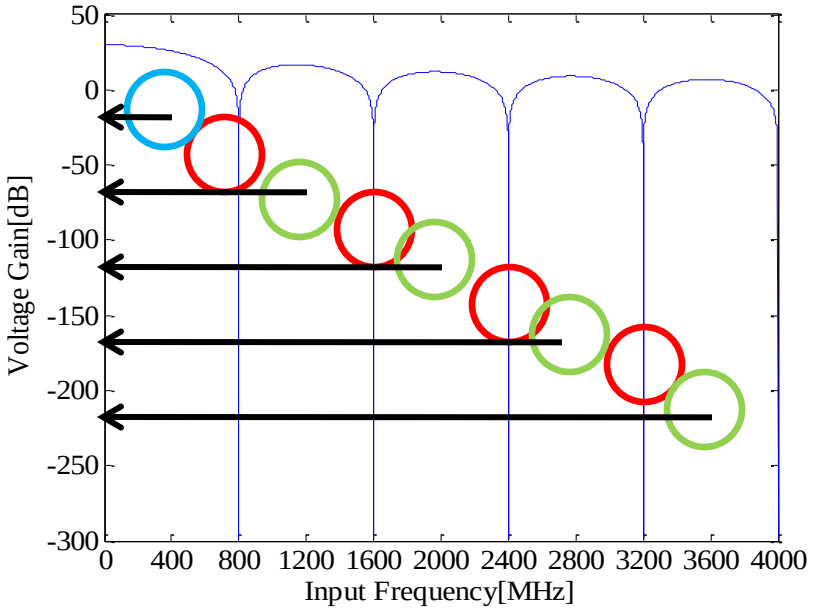
Current Integration Sampling



$$C_S V_S = \int_0^{\frac{T_{LO}}{2}} g_m V_{\text{in}} e^{j\omega t} dt$$

$$= \frac{g_m}{\pi f} \cdot e^{j\omega\left(\frac{T_{\text{LO}}}{4}\right)} \cdot \sin\left(\frac{\pi f T_{\text{LO}}}{2}\right) \cdot V_{\text{in}}$$

$$\left|H_{CI}\right| = \left|\frac{V_S}{V_{\text{in}}}\right| = \frac{g_m T_{\text{LO}}}{2C_S} \cdot \left|\text{sinc}\left(\frac{\pi f T_{\text{LO}}}{2}\right)\right|$$



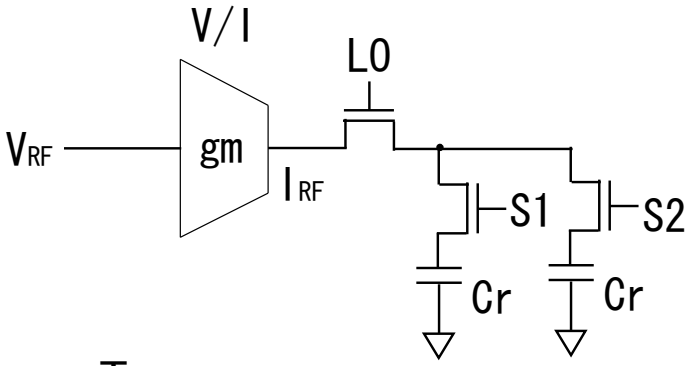
←fLO=400MHz

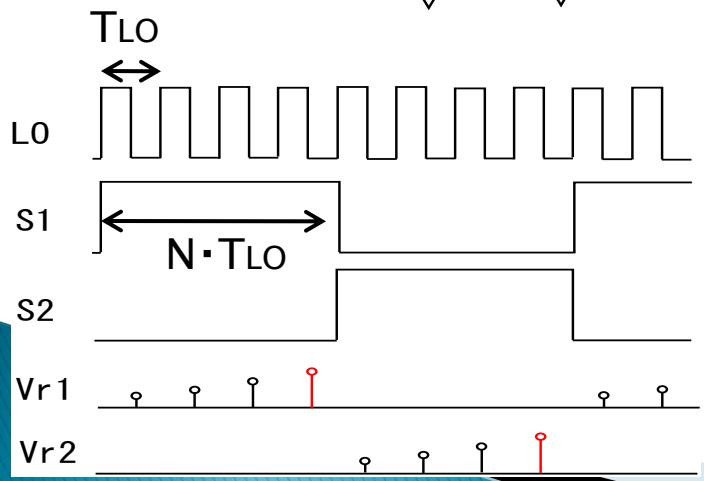
CIS performs as sinc filter.
Interferences and holding noise from even frequency can be suppressed.

However, Output rate (= fRF) is too fast.
For ADC, decimation is needed.

Decimation (FIR)

- Use two rotating capacitor C_R
- Accumulate the charge N times
- Output rate = $f_{RF}(=f_{LO})/N$



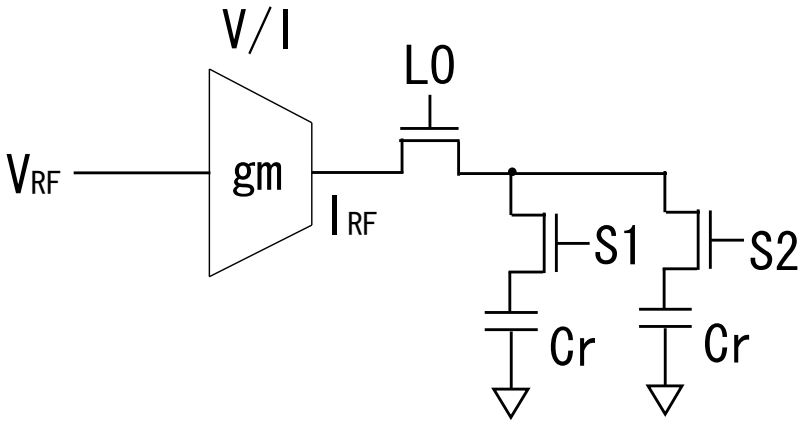


$$C_R V_S\left(1+z^{-1}+z^{-2}+\cdots+z^{-(N-1)}\right)=C_R V_R$$

$$H_1 = \underbrace{H_{CI}}_{\text{sinc}} \cdot \underbrace{\frac{1-Z^{-N}}{1-Z^{-1}}}_{\text{FIR}}$$

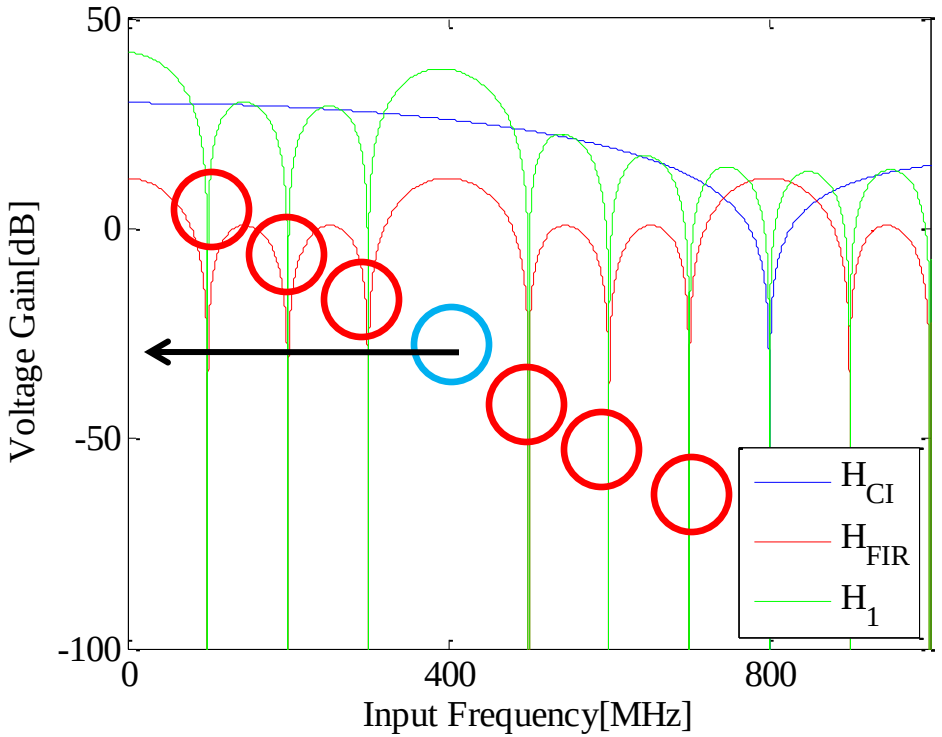
FIR filter can be achieved by charge accumulation.

Decimation (FIR)



$$H_1 = H_{CI} \cdot \frac{1 - Z^{-N}}{1 - Z^{-1}}$$

sinc FIR



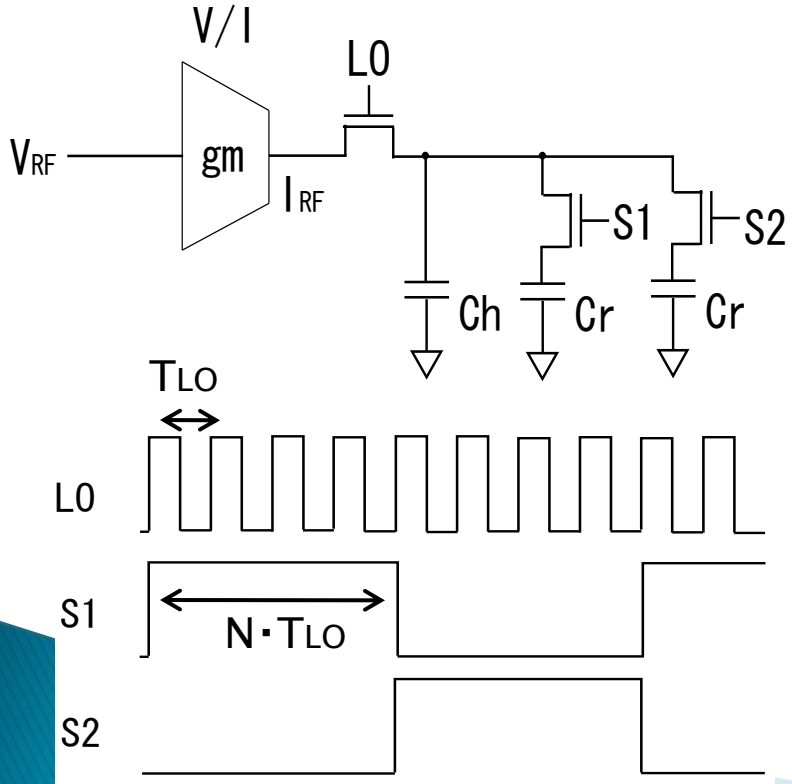
f_{LO}=400MHz, N=4

Charge accumulation performs as not only decimation, but also FIR (anti- aliasing) filter.

However, filter characteristics is not enough for channel selection.

Charge sharing (IIR)

- Add history capacitor C_H
- In contrast to C_R, C_H is not reset.
- At the moment when S1 or S2 become on-state, C_H shares the charge with C_R.



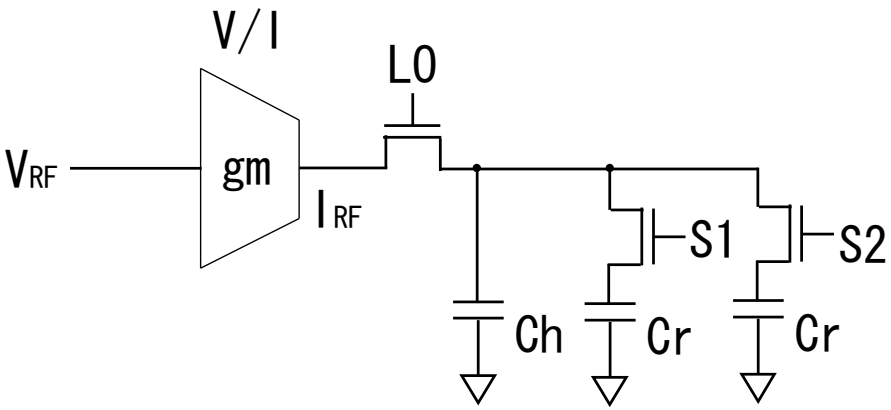
$$(C_H + C_R)V_1 + C_H z^{-N} V_{IIR1} = (C_H + C_R)V_{IIR1}$$

$$H_2 = H_{CI} \cdot H_{FIR} \cdot H_{IIR}$$

$$H_{IIR1} = \frac{1}{1 - \frac{C_H}{C_H + C_R} z^{-N}}$$

IIR filter can be achieved by charge sharing.

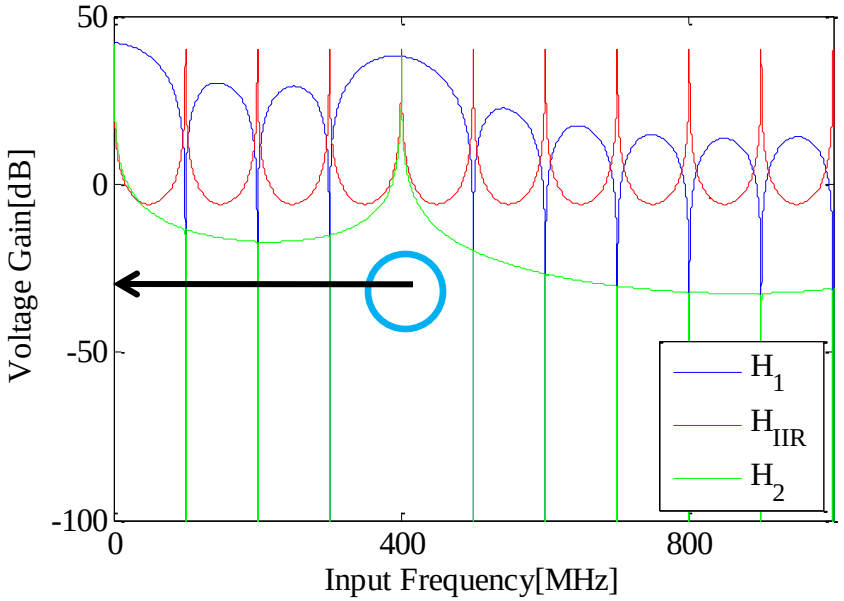
Charge sharing (IIR)



$$H_2 = H_{CI} \cdot H_{FIR} \cdot H_{IIR}$$

Sinc × FIR　　IIR

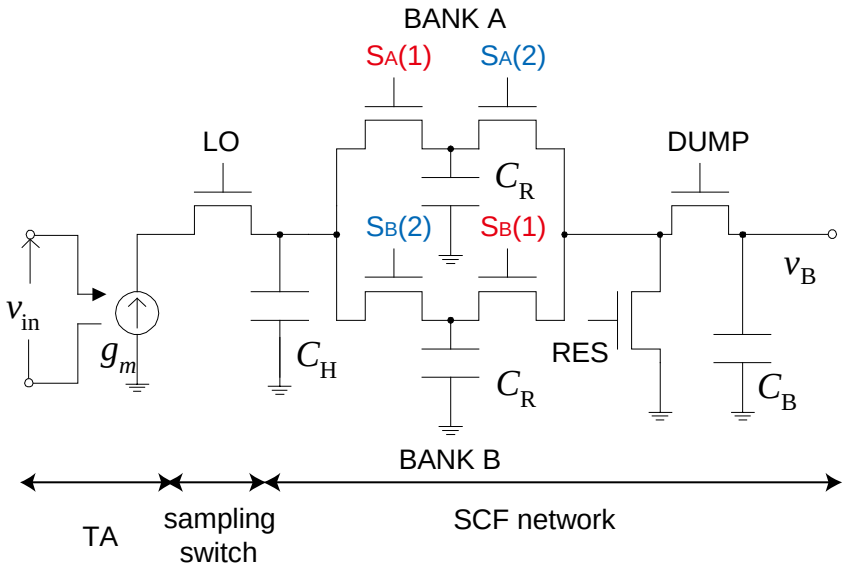
$$H_{\mathrm{IIR}} = \frac{1}{1 - \frac{C_{\mathrm{H}}}{C_{\mathrm{H}} + C_{\mathrm{R}}} z^{-N}}$$



fLO=400MHz, N=4

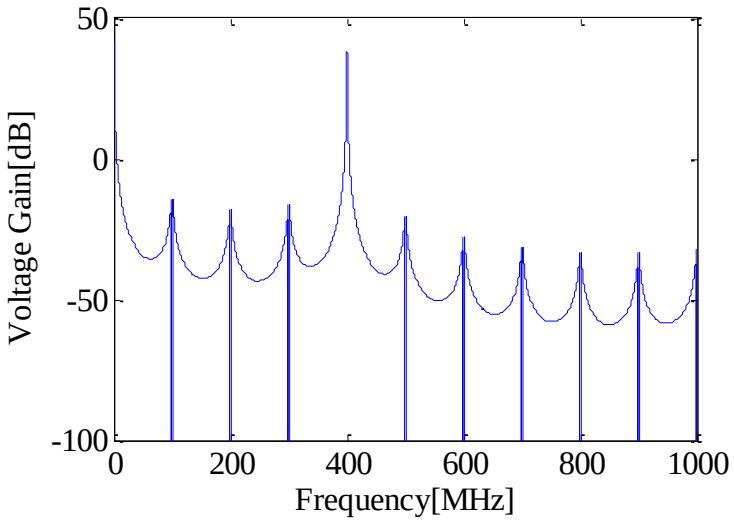
Chanel selection can be achieved by charge sharing IIR filter.
Bandwidth is defined by capacitance ratio.

Architecture and Feature of DSM



$$H_{\mathrm{DSM}} = H_{CI} \cdot H_{\mathrm{FIR1}} \cdot H_{\mathrm{IIR1}} \cdot H_{\mathrm{IIR2}}$$

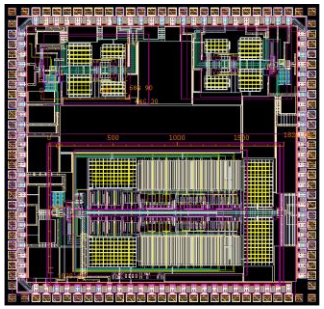
$$H_{IIR2} = \frac{C_R}{C_R + C_B} \cdot \frac{1}{1 - \frac{C_B}{C_R + C_B} z^{-N}}$$



- CMOS performs as a switch.
- Direct Down conversion by charge sampling (no IF)
- Relaxation of the performance requirement of ADC by decimation and filtering
- Reconfiguration by changing capacitor set and clock frequency, architecture.

Issues and Objectives

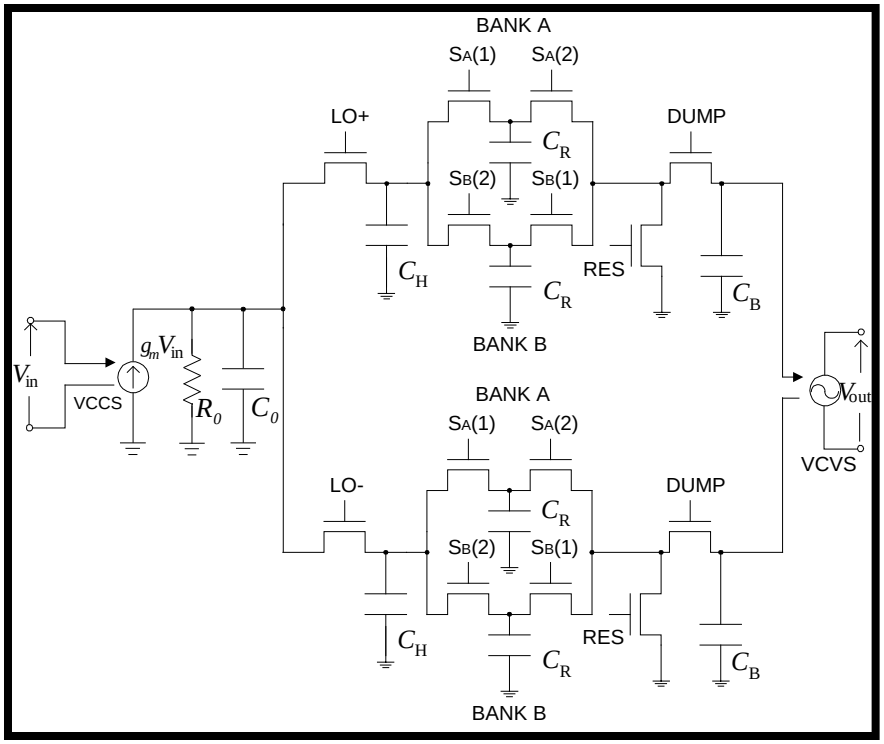
- Noise Figure (NF) of DSM measured from our prototype is over 20dB.
- Gain of CMOS LNA is around 10dB.
- Noise component from DSM can not be negligible.



- Analyzing the noise characteristics of DSM
- Designing the low noise DSM

Noise analysis of SCF circuit

Noise from MOS switches in SCF networks is analyzed.

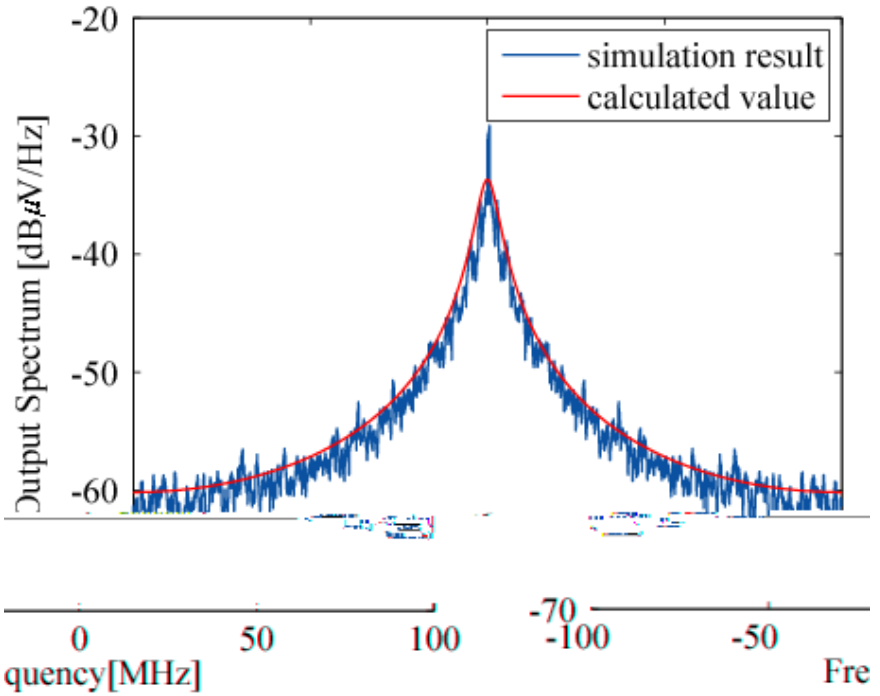


Simulation parameter

f_{LO}	g_m	R_0	C_0
400MHz	10mS	41Ω	3.2pF

0.18 μm MOS model from TSMC is used.
Switches consist of nMOS.

Simulation result



Calculated value shows good agreement with simulation result.
The noise level is in inverse proportion to capacitance value.
In practical parameter, noise components from TA is dominant.

Noise Figure (NF) of DSM

- Assuming that noise from TA is dominant,

$$F_{DSM}(f)=\frac{SNR_{in}(f+f_{LO})}{SNR_{out}(f)}=\frac{N_{out}(f)}{G(f+f_{LO})N_{in}(f+f_{LO})}$$

$$\cong 1+\frac{N_{TA}(f+f_{LO})}{GN_{in}(f+f_{LO})}=1+F_{TA}(f+f_{LO})$$

N_{TA} :internal noise from TA

F_{TA}:noise factor of TA

- Including buffer circuit which is located in next stage,

$$F'_{DSM}(f)=F_{DSM}(f)+\frac{F_{buffer}(f)-1}{G(f)}$$

F_{buffer} :noise factor of buffer

G :gain of DSM

- In prototype which was made in 2006, noise characteristics deterioration is caused by gain degradation.

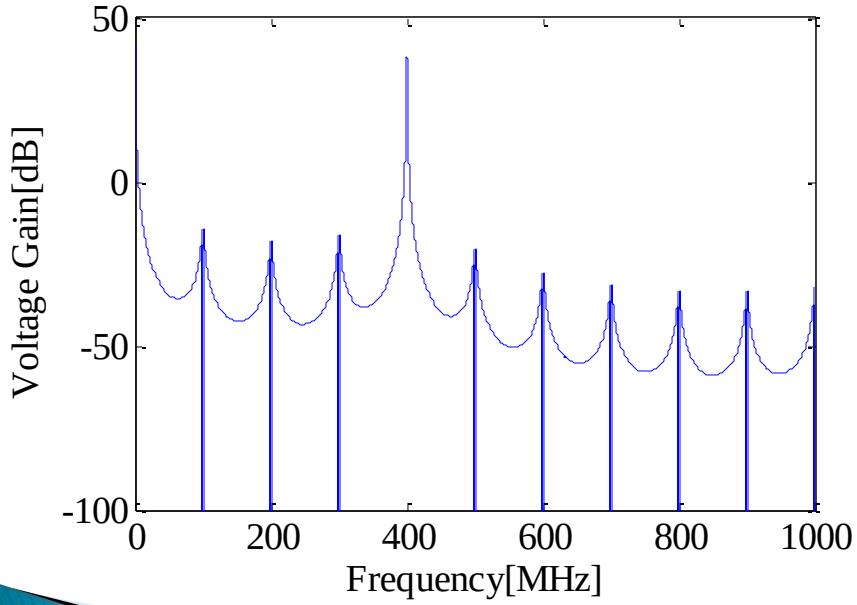
Conclusion

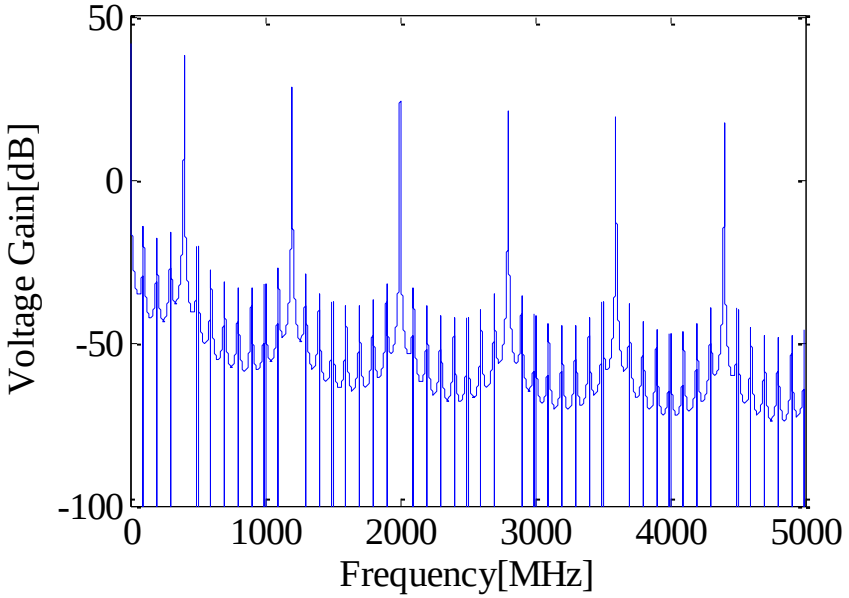
- DSM can realize a reconfigurable RF circuit, and is suitable for CMOS technology.
- However, some issues are remained.
  noise characteristics, nonlinearity,
  variety of filtering characteristics ..
- To achieve low NF, it is necessary to improve the gain of DSM.

Appendix

Frequency Characteristics

f_{LO}=400MHz, N=4
C_H=20pF, C_R=0.2pF, C_B=2pF

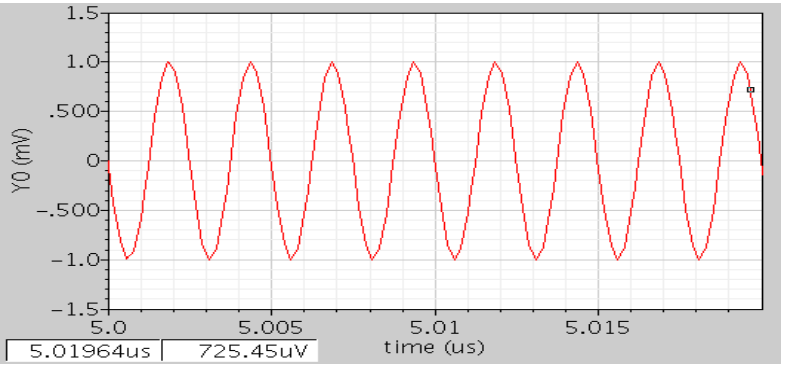




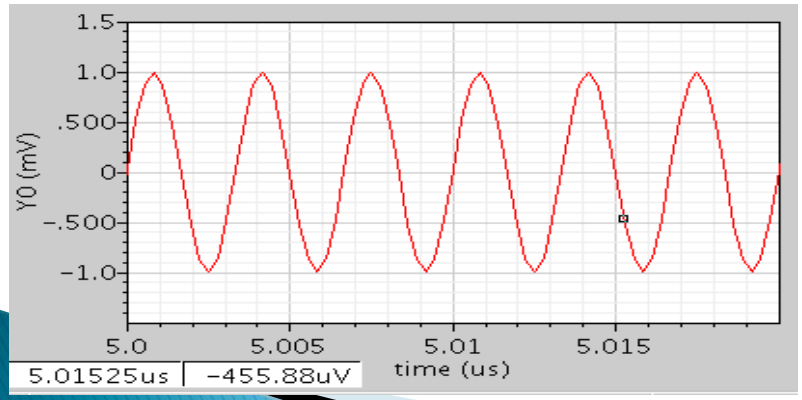
Filter embedded Mixer

Input

400.5MHz



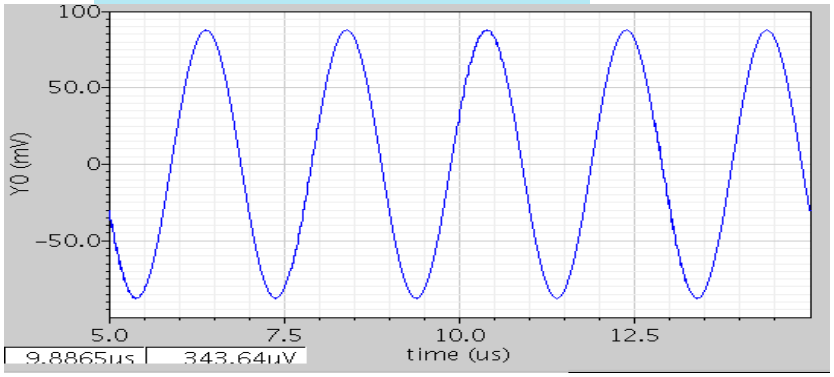
300MHz



f_{LO}= 400 MHz

Output

500kHz
Voltage Gain=39dB



100MHz
Voltage Gain=-21dB